

# Over 10Gbps transmission

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# Session Agenda & Objectives

- **Introduction to Signal Integrity Issues**
  - Where does loss come from
  - How materials effect transmission characteristics
  - Impedance discontinuities
- **Signal Conditioning Techniques**
  - EQ / Pre & De-Emphasis
  - Advanced SigCon techniques (DFE)
  - Retiming to remove random jitter
- **Tips**
  - Applications & Solutions
- **Summary**
- **Appendix**

## Session Objectives:

- Become familiar with where loss comes from
- Understand various SigCon features
- Identify Solutions for common problems

# Introduction to Signal Integrity Issues

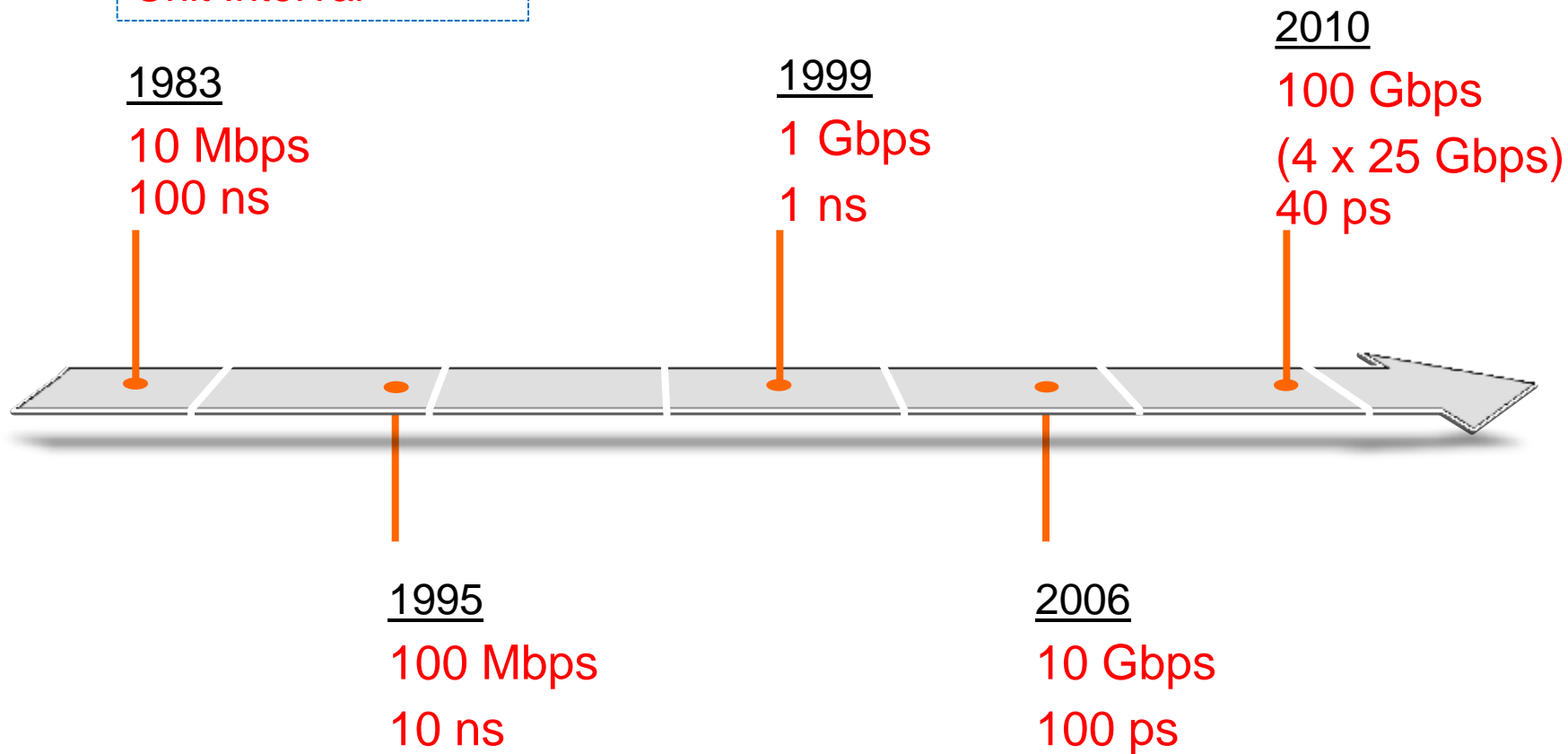
Subhead text here

# Progression towards 100Gbps....

Year standardized

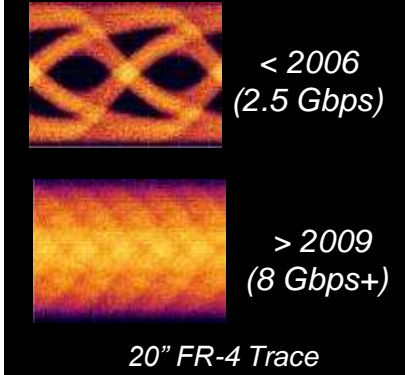
Data Rate

Unit Interval



# Interface Challenges

**1**



< 2006  
(2.5 Gbps)

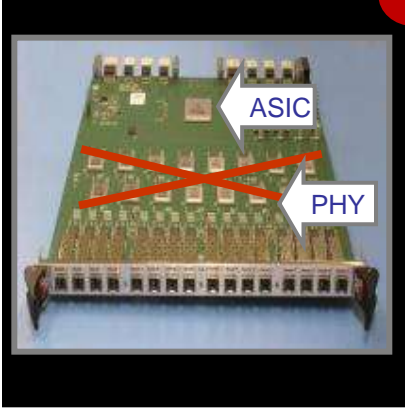
> 2009  
(8 Gbps+)

20" FR-4 Trace

Doubling Data Rate,  
Reach Remains Same

Signal / Noise Problem

**2**



ASIC

PHY

Shrinking CMOS Cells,  
PHY Integration,

Jitter Problem

**3**



Higher Density,  
Chassis Life Extension

Cross Talk Problem  
Power Density Problem

**4**



PCI EXPRESS

SERIAL ATA

ETHERNET

Serial Attached SCSI

Plethora of Standards,  
Complex Designs

Time-to-Market Problem

# Doubling Data Rate, Reach Remains Same

*Signal Integrity Problem Growing*

Doubling Data Rates, Reach Remains Same

Changing System Architecture

Design Expertise

< 2009

2010

> 2010

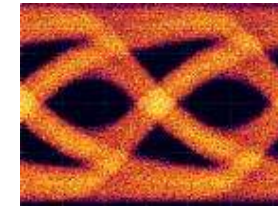
*What happens to high speed signals after 26" of board trace?*

Local Area Network (LAN)

1 Gbps

10 Gbps

100 Gbps



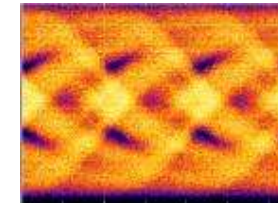
< 2006  
(2.5 Gbps)

Server I/O

PCIe 2.5G

PCIe 5G

PCIe 8G



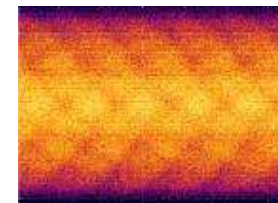
2006-2009  
(5 Gbps)

Storage Area Network (SAN)

FC 4G

FC 8G

FC 16G



> 2009  
(8 Gbps+)

CPRI

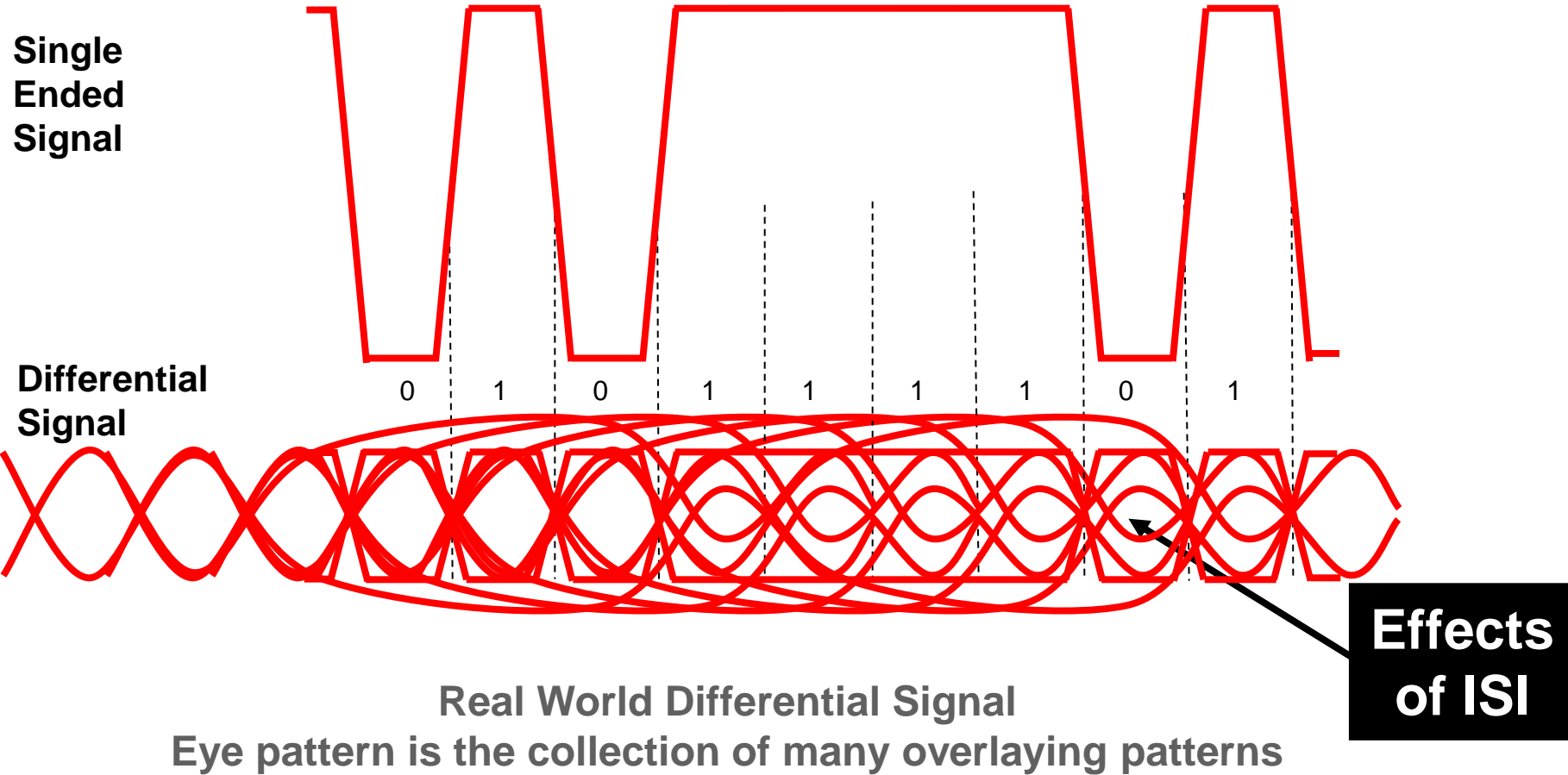
3 Gbps

6 Gbps

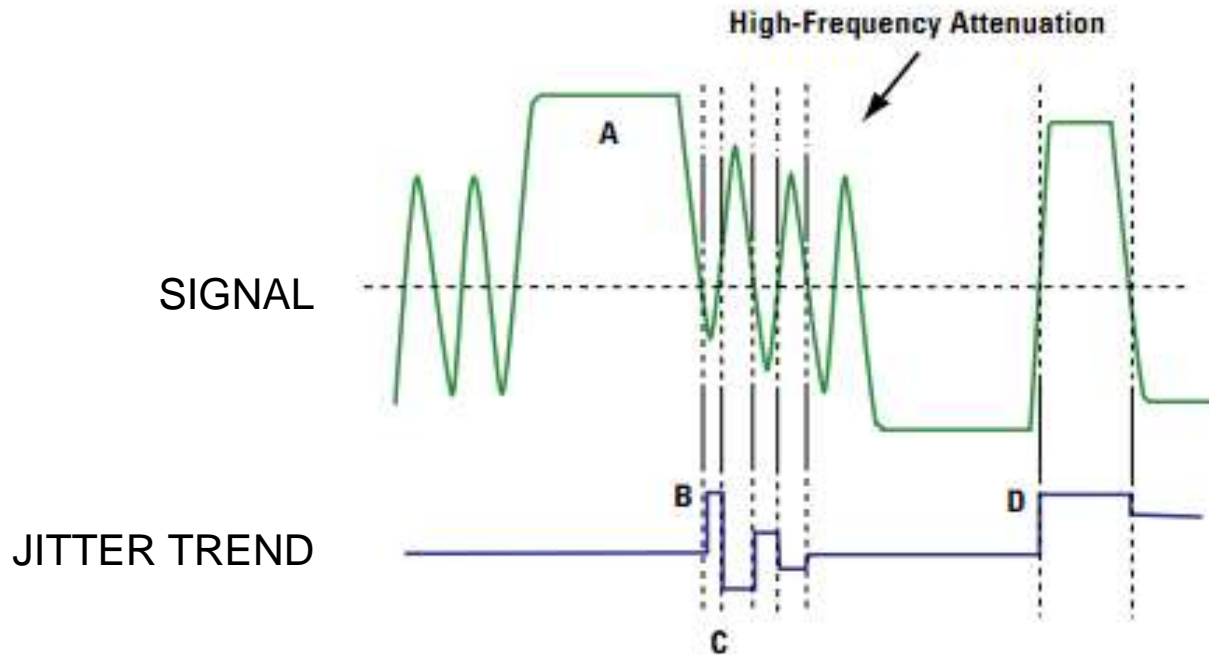
9.8 Gbps

# Single Ended vs Differential

## *Inter Symbol Interference (ISI) and LOSS*



# Inter-Symbol Interference (ISI) Jitter



- ISI is data pattern dependant and is effected **by the history of the stream**
- **Longer run lengths** (i.e. PRBS-31) will tend to have **more ISI** if bandwidth is limited
- The “jitter trend” curve above shows how the pattern effects the jitter
- **Reflections complicate** the matter and add JITTER (not shown)

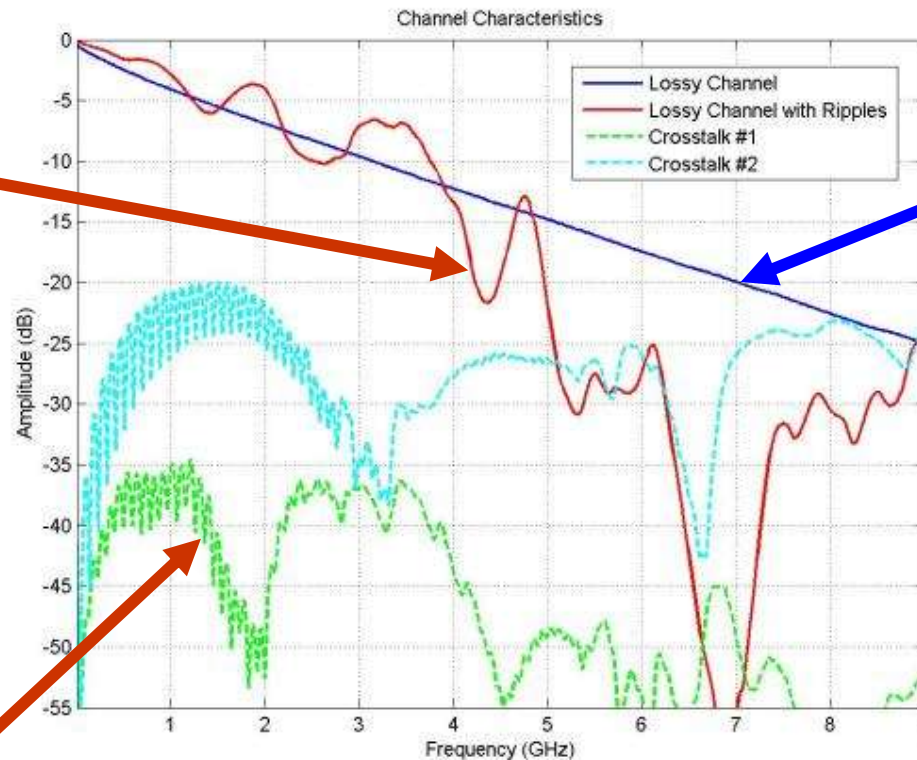


# Transmission Loss Profile

*Linear loss, Resonance, Reflections, X-talk*

Ripples – Impedance discontinuities

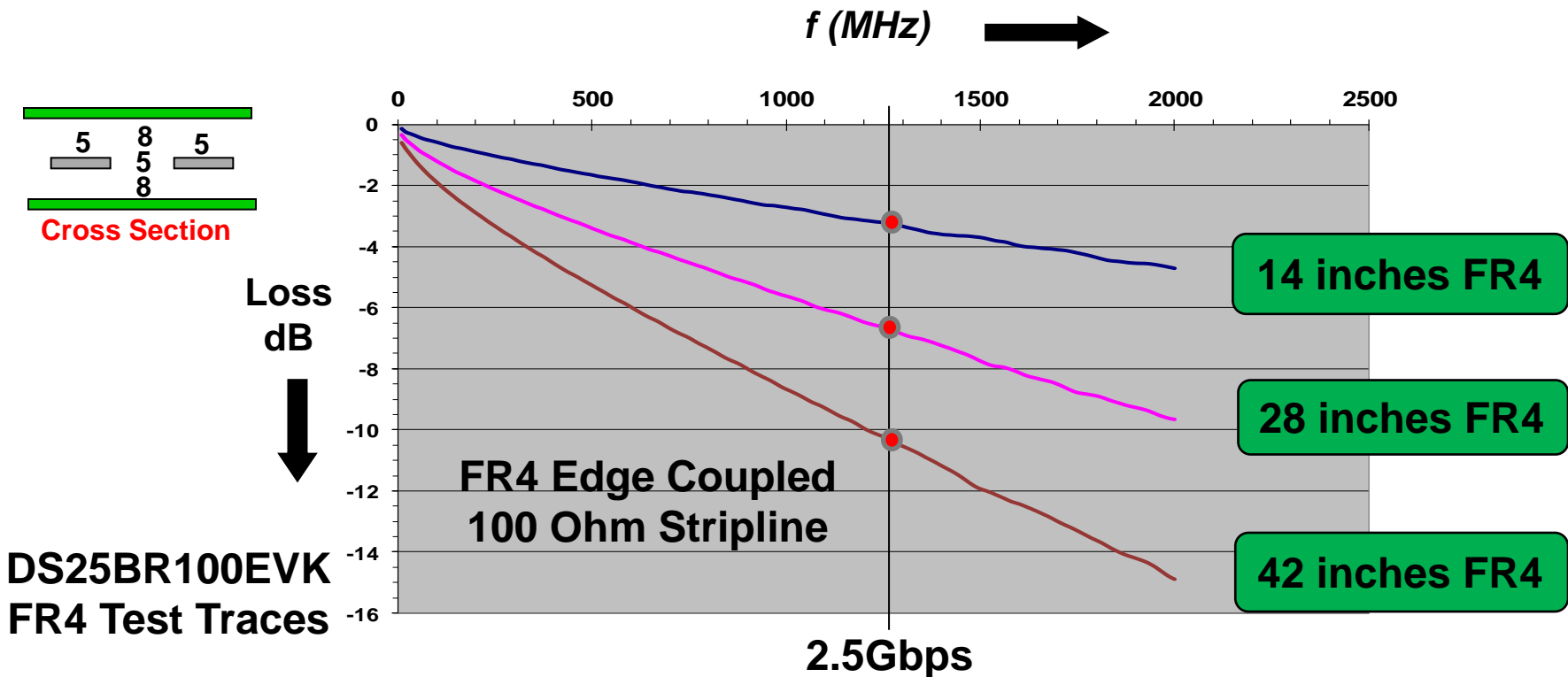
Linear Loss



Choppy – Crosstalk

# Where does LOSS come from?

## FR4 Loss vs. Length vs. Frequency



- Loss proportional to  $\text{SQRT}(f)$  (copper losses) and  $f$  (dielectric losses)
- Depends on transmission line geometries
- Depends on material properties

# Common PCB Materials

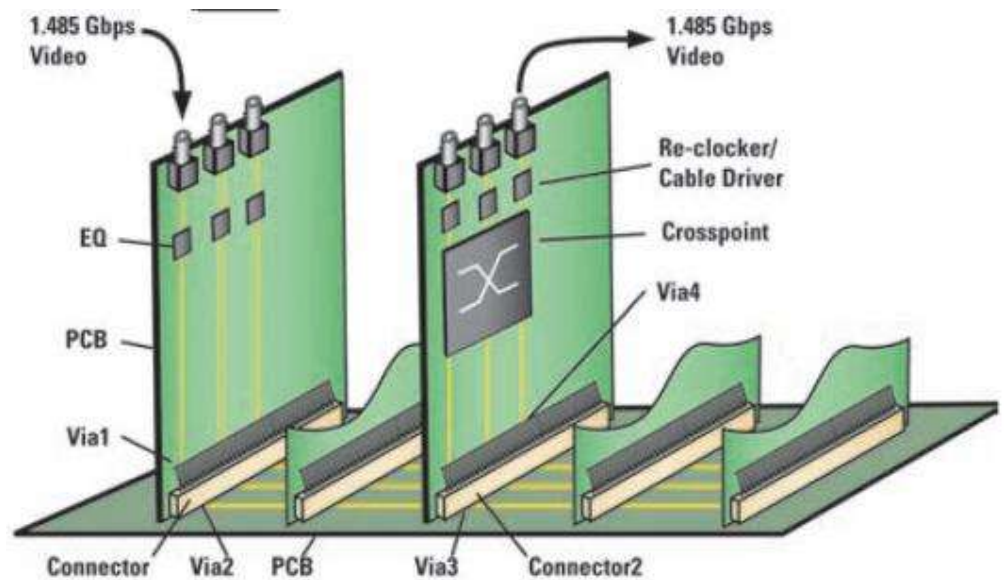
- Better materials have low dielectric constants that are flat with frequency
- More exotic materials have lower loss, thus providing better signal quality over the same distance or longer reaches

Name	Material	Dk (1MHz)	Dk (1GHz)	Dk (10GHz)
FR-4	GE	5.25	-	4.10
Nelco 4000-13	GE (Mod)	-	3.70	3.60
Hitachi FX-II	PTFE	-	3.60	3.40
Panasonic Megtron-6	PTFE	-	3.40	3.40

\* PTFE: Polytetraflouroethylene (Teflon), GE: Glass Epoxy

# Overcoming Impedance Discontinuities

- As signals propagate from board-to-board through traces, feed-thru's and connectors, there are inevitable impedance discontinuities
- A TDR evaluation will highlight these discontinuities
- Careful layout, connector selection, and circuit board materials all factor into maintaining a relatively constant characteristic impedance

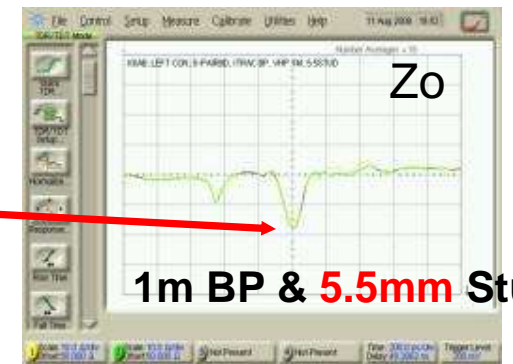
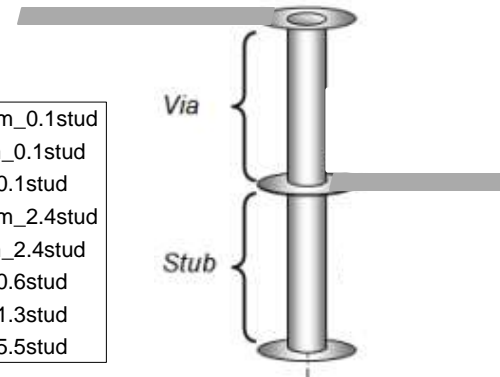
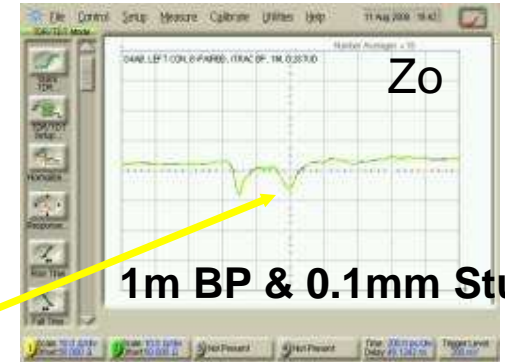
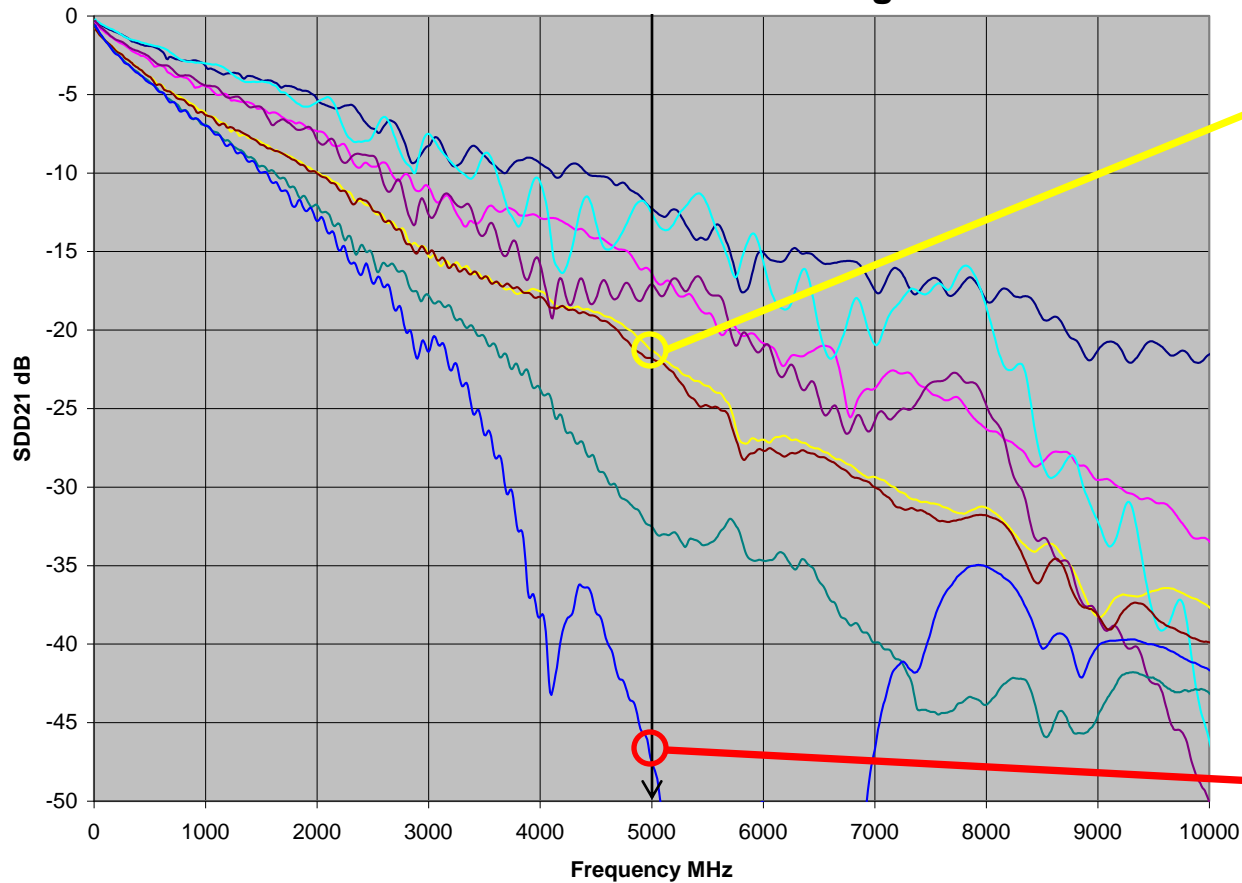


L  
C

# 10G Design Considerations

## Stubs matter

Molex iTrac Backplane  
1m vs VIA stub length



# Crosstalk – FEXT & NEXT

Crosstalk contributes to periodic jitter that can degrade system performance

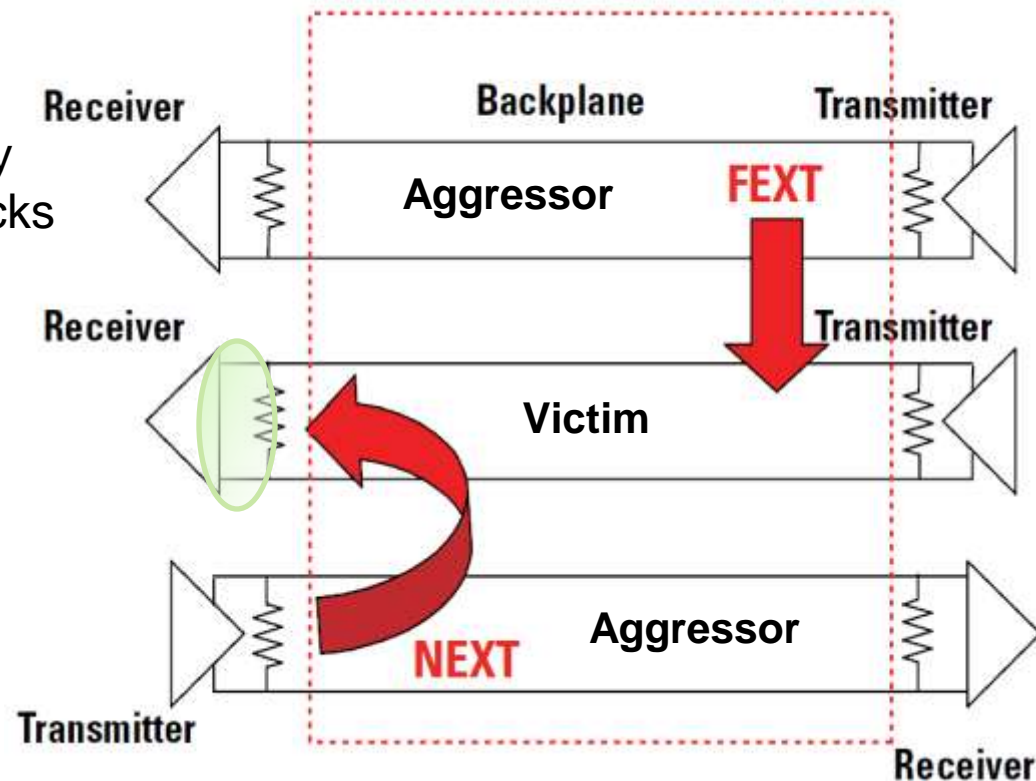
- Crosstalk is interference caused by adjacent data channels and/or clocks

## Far-End Crosstalk (FEXT)

- Crosstalk noise is injected into the victim channel at the far end of a channel and is measured at the receiver

## Near-End Crosstalk (NEXT)

- Crosstalk noise usually from an adjacent transmitter is injected at the receive end and is measured at the receiver



*Far-End & Near-End Crosstalk Examples*

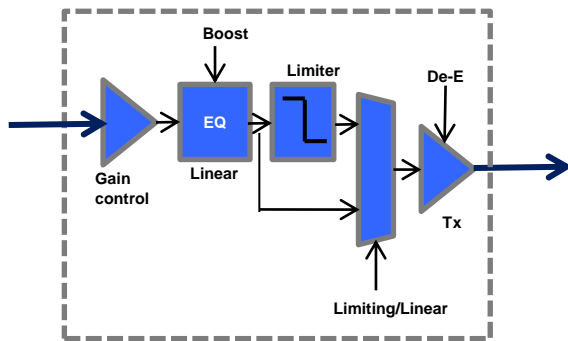
# Signal Conditioning Techniques

Subhead text here

# Right Tool for The Right Job

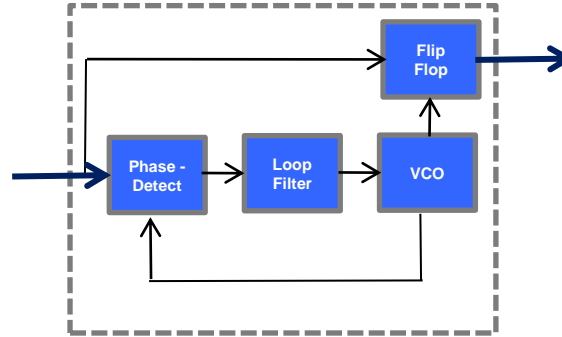
## Redrivers, Retimers, and Advanced SigCon

### Equalization & De-Emphasis Driver



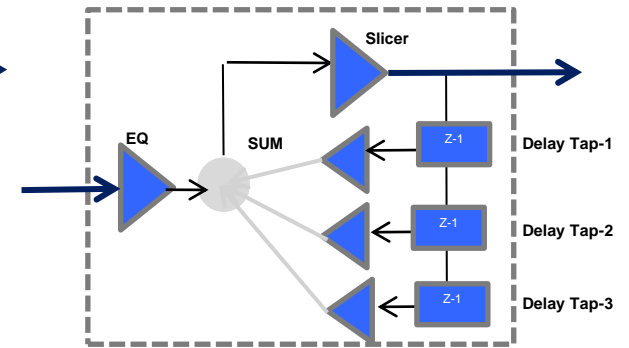
✓ Insertion Loss

### Clock Data Recovery (CDR)



✓ Jitter

### Decision Feedback EQ (DFE)

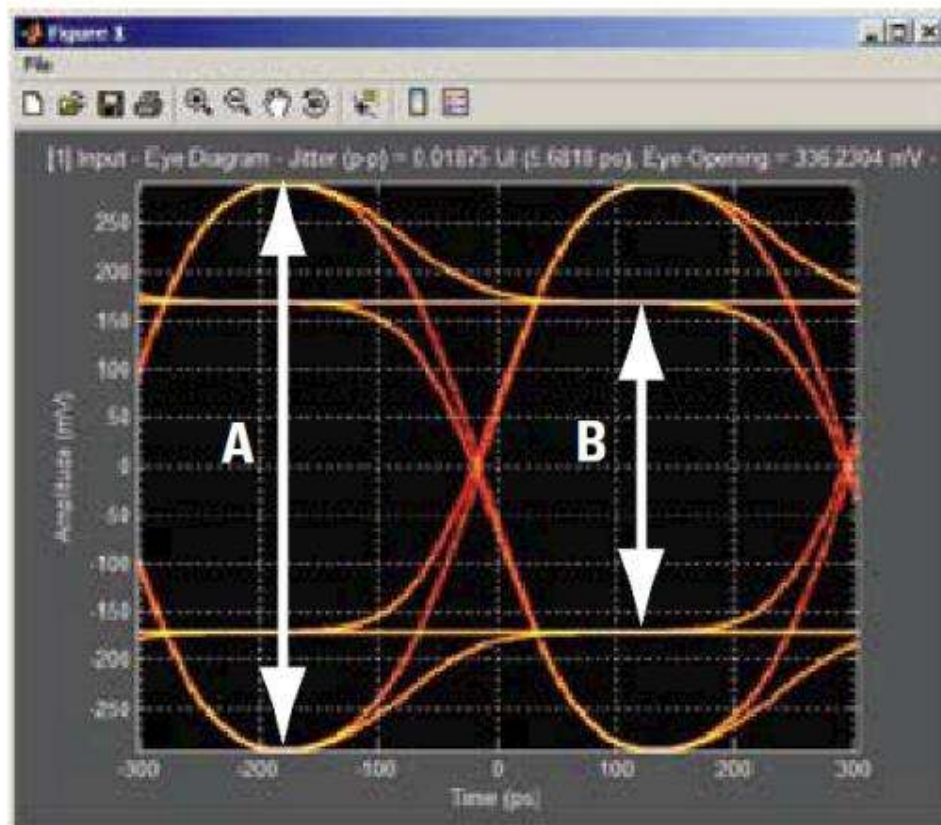


✓ X-Talk, Reflections



# Signal Conditioning: PE and DE

- Pre-Emphasis & De-Emphasis techniques address high frequency media loss by applying a frequency-selective boost or attenuation component to the data at the transmit end
- **Pre-Emphasis (PE)**
  - Edge energy is boosted by creating an overshoot on every edge
  - Typically used with LVDS
- **De-Emphasis (DE)**
  - Edges are kept the same, but the settled amplitude is attenuated
  - Typically used with CML

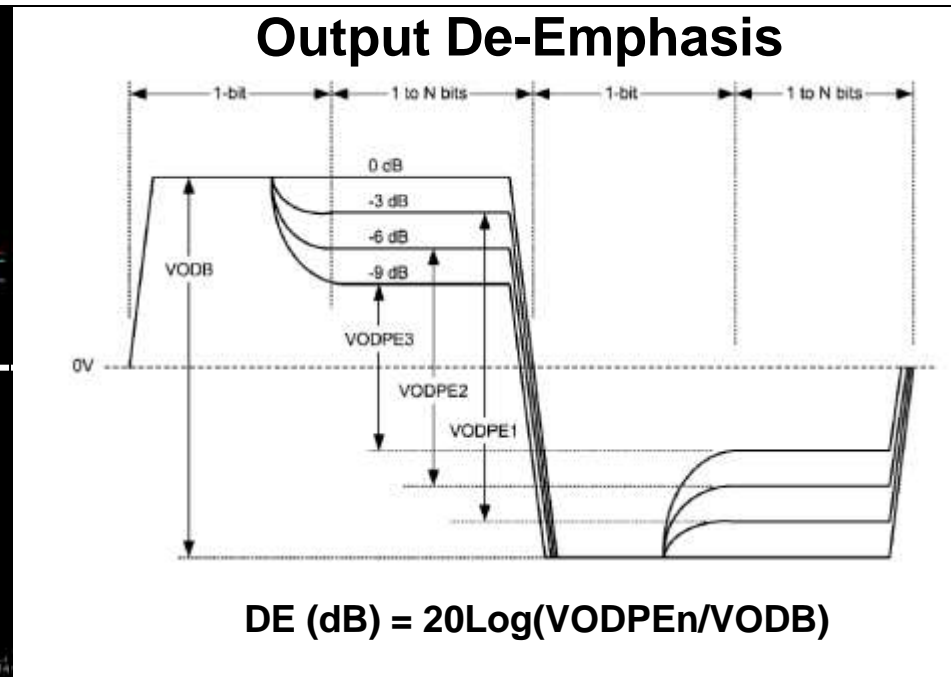
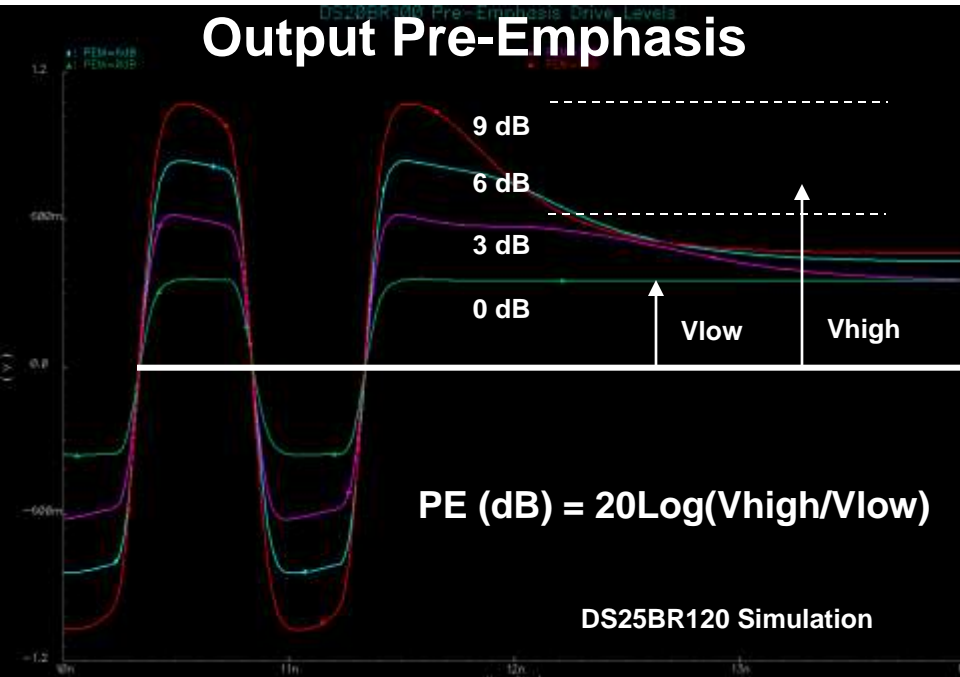


$$PE = 20 \times \log_{10}(A/B): \text{Transmit } V_{OD} = B$$

$$DE = 20 \times \log_{10}(B/A): \text{Transmit } V_{OD} = A$$

# Transmit Signal Conditioning Explained

## Pre-Emphasis (Pre-E) vs De-Emphasis (De-E) Waveforms



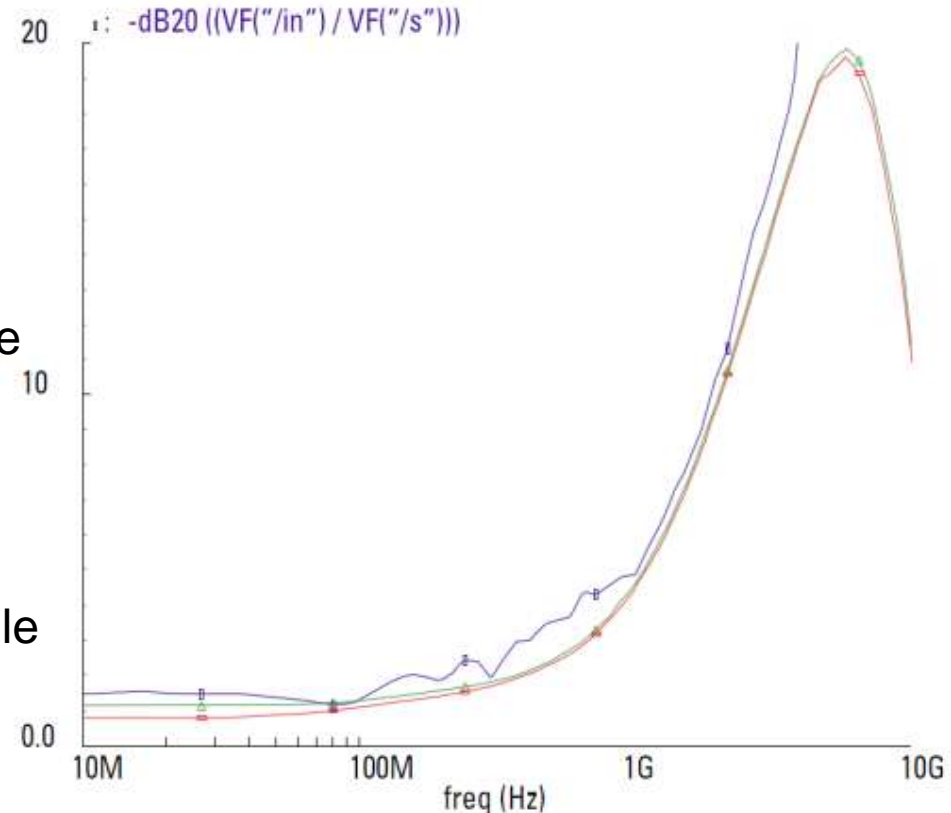
0	1	0	1	1	1	1	1	DATA	1	1	0	0
PATTERN												

**Pre-E Tends to be used with LVDS**  
**Single direction – Longest links**

**De-E Tends to be used with CML**  
**Low EMI, Low Power, Bidirectional**  
**Shorter**

# Signal Conditioning: Receive Equalization

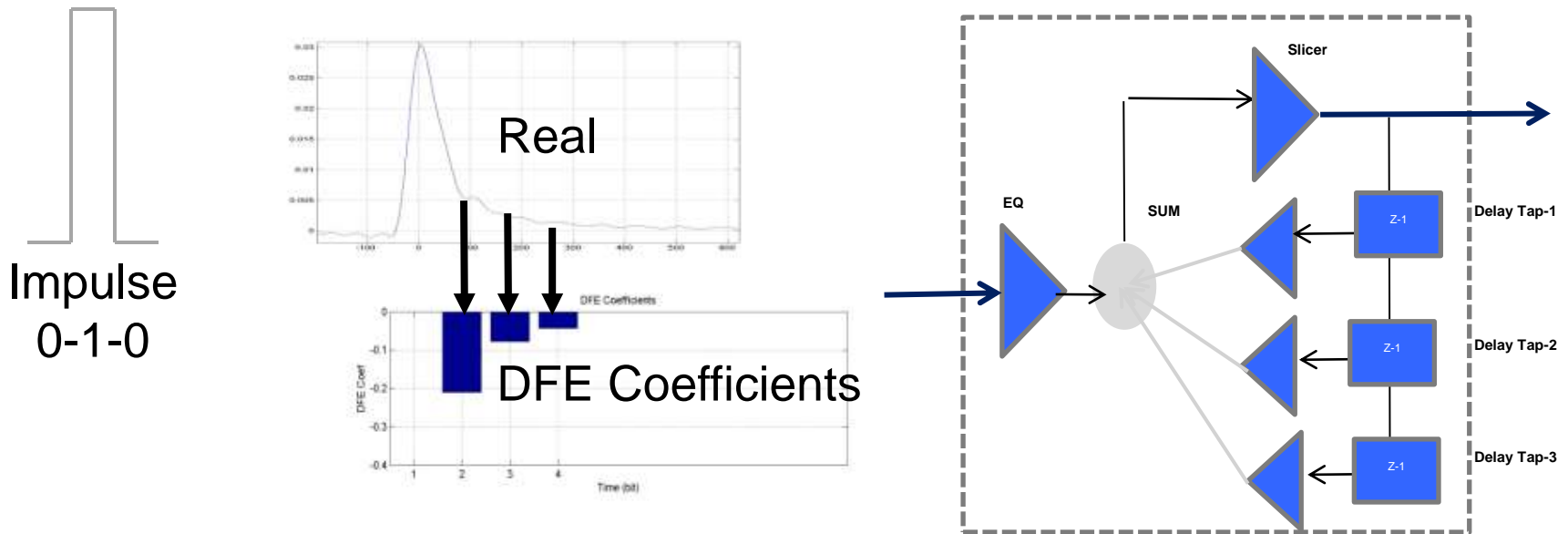
- **Equalization is applied at the receive end**
  - Selectively boosts high-frequency data
  - Compensates for the media's high frequency roll-off
  - Includes a high-pass filter that ideally has a frequency response exactly opposite to the media loss that the equalizer is attempting to compensate
  - Equalizers may be active or passive; fixed, variable or adaptive
- **Active Equalizers**
  - Can add gain to high frequencies while attenuating low frequencies
  - Works best with low-level signals
  - Can often be “programmable” or “adaptive”



*Inverse Channel Response (blue) and Matching Equalizer Response (green)*

# Advanced SigCon

## Decision Feedback Equalizer (DFE)

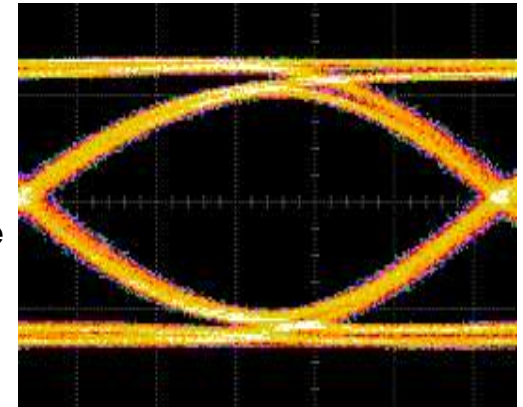


- Helps to **open** the EYE in the amplitude domain to **reduce BER**
- Counters impact of **X-Talk** and **Reflections**
- Useful at the higher data rates where every ps matters most
- **Eye Openers**
  - **Equalizers** reduce Jitter in the X axis to open the **EYE**
  - **DFEs** reduces amplitude noise in the Y axis to open the **EYE more**

# Eye-Opening Monitor (EOM)

- **Many Uses:** prototype, lab, factory test, remote diagnostics, Figure of merit (FOM) and more!
- **Signal Fidelity** measurement where it matters without probing effects, HEO, VEO (reg value)
- Featured on most high-speed **RETIMER** and **DFE** based **Advanced SigCon** solutions

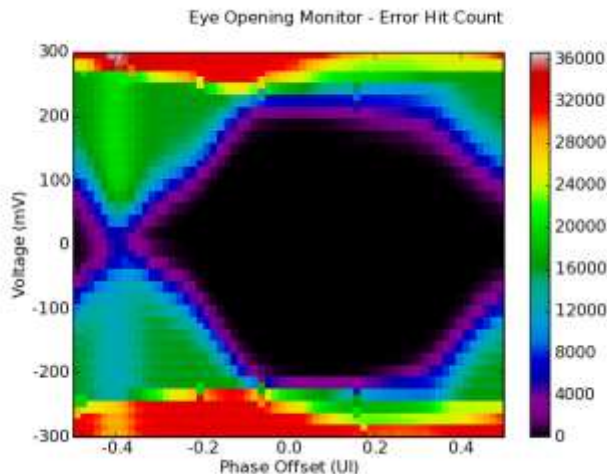
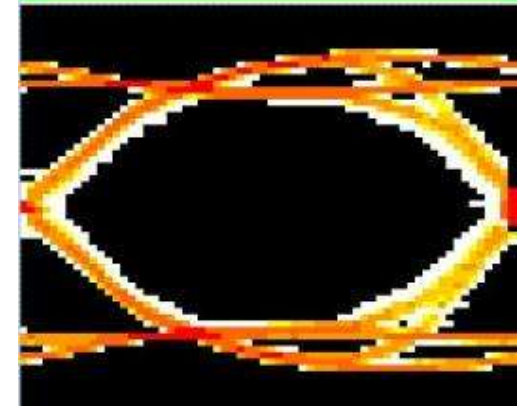
Lab Data from Sampling Scope



Internal Eye Monitor Raw Hits



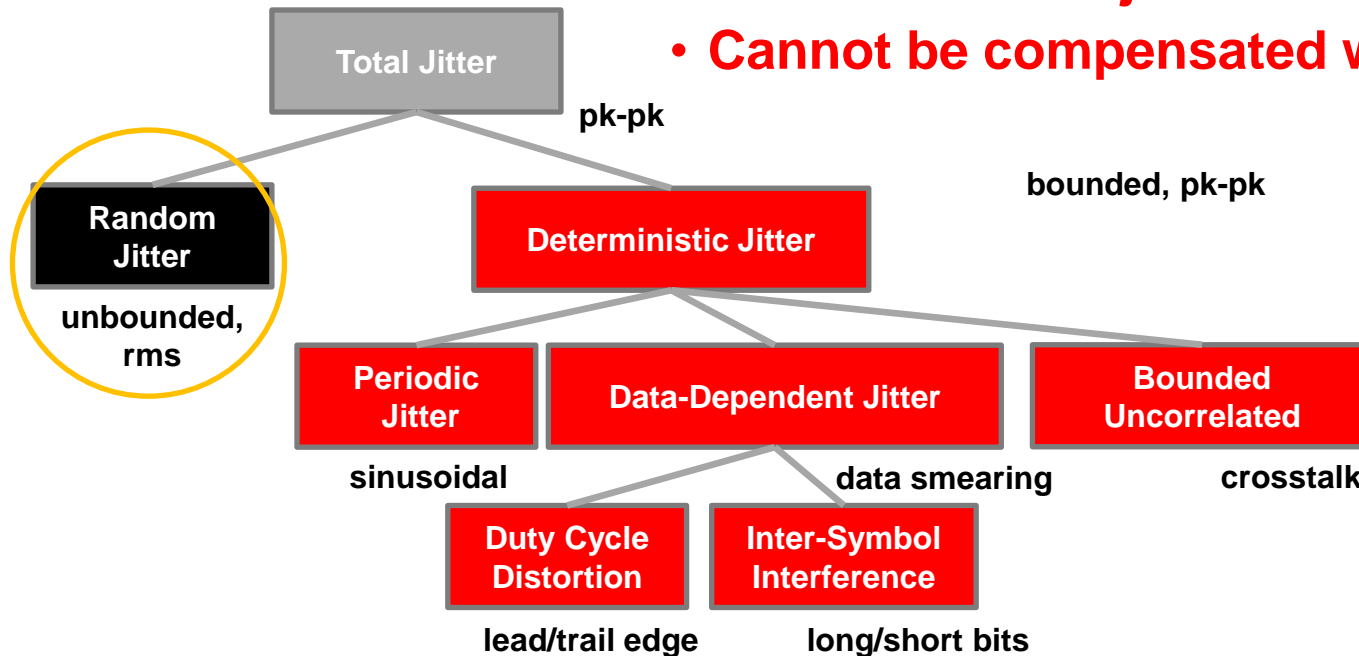
Density of Hits



10G, 100ps, 1.5ps & 6mV resolution

# Random Noise and Jitter Revisited

- Random noise / jitter is not predictable
- Cannot be compensated with equalization

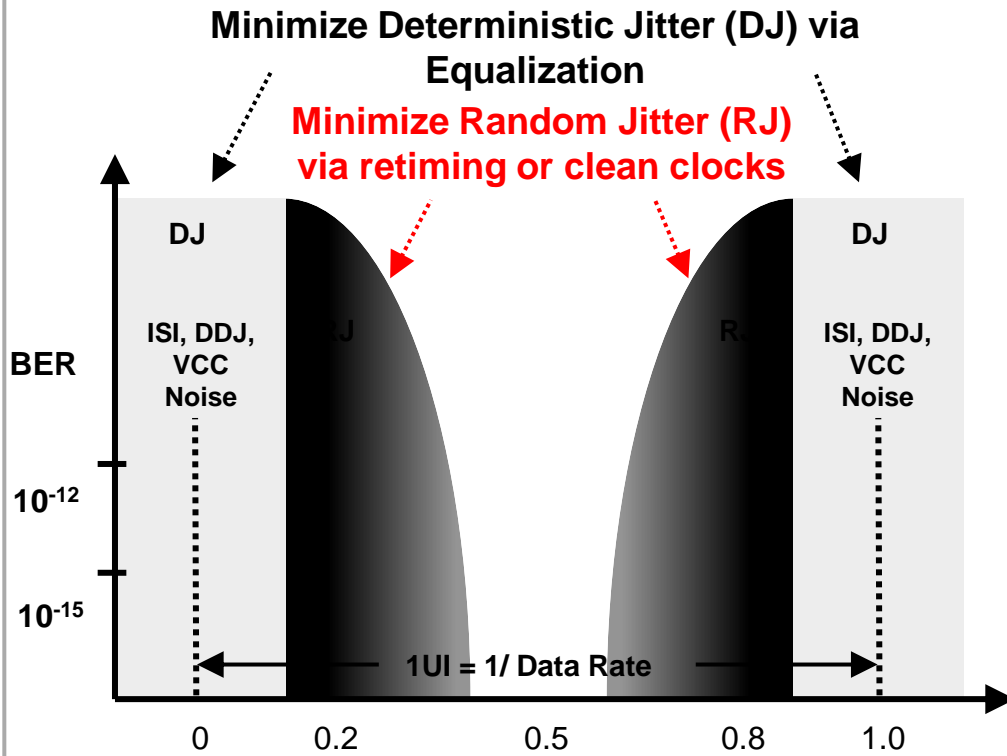


- Results from the random nature of electrons and the random obstacles that the electrons overcome as they carry info down electrical channels
- Gaussian in nature
- 3 main system Components: driver jitter, channel jitter, and receiver jitter



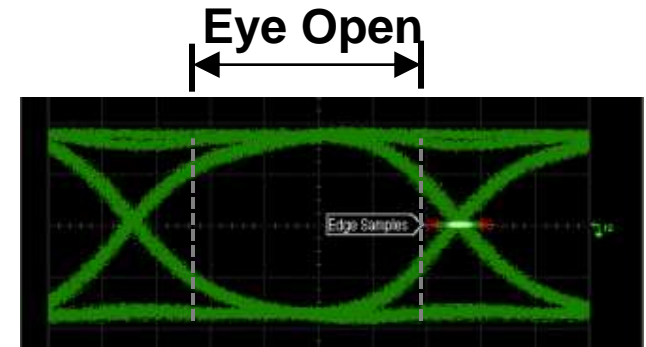
# Jitter Limits Performance

## Bathtub Curve Performance

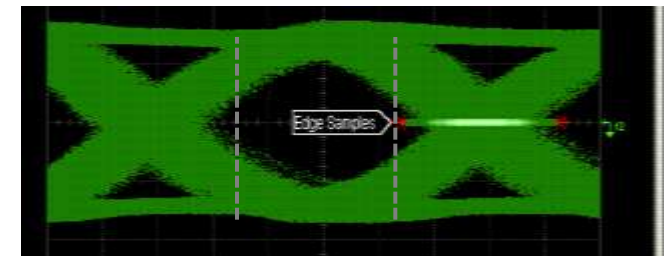


*Random jitter reduces the eye opening*

## Scope Results

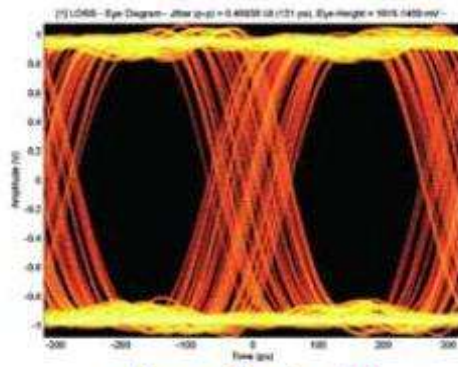


*Eye closing due to jitter*

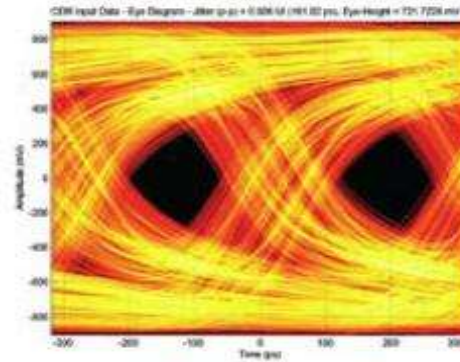


*Clock jitter is a critical requirement in high speed communications*

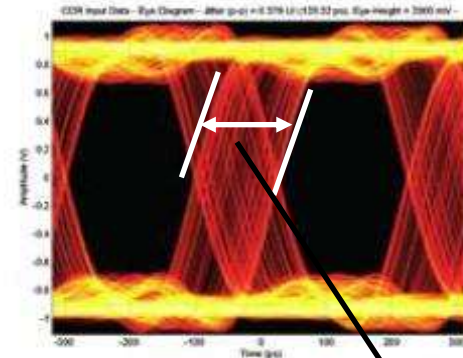
# Using Re-timers to Overcome RJ



a) Input Clock with 0.4 UI Jitter @ 20 MHz

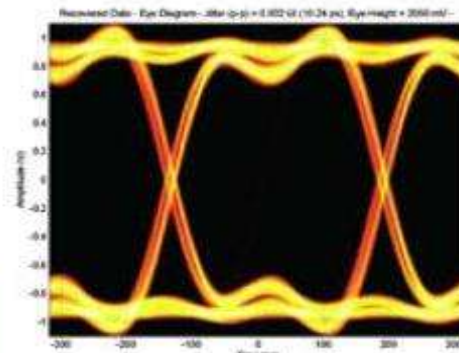


b) After Channel

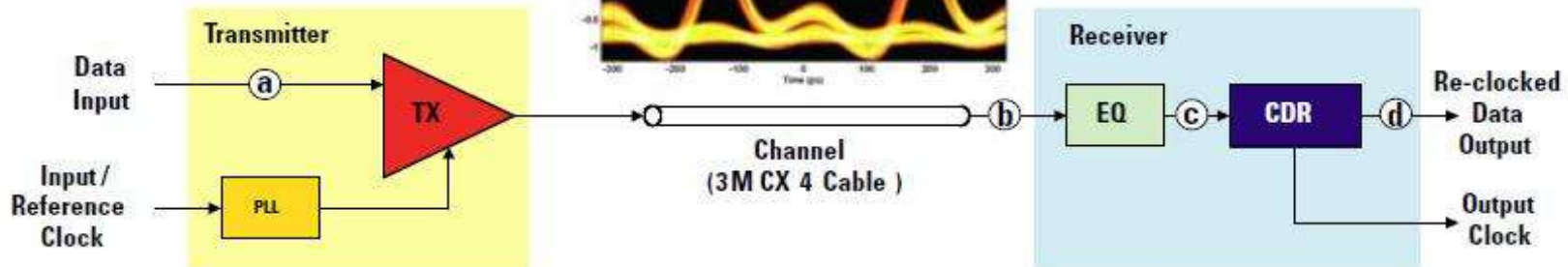


c) After Equalizer

Residual Jitter Left by EQ



d) After Re-clocking



Helps with minimizing Random Jitter (RJ), crosstalk, reflection, and residual Deterministic Jitter (DJ) in a channel



# Tips

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# Today's Tips

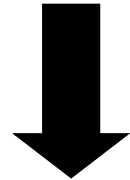
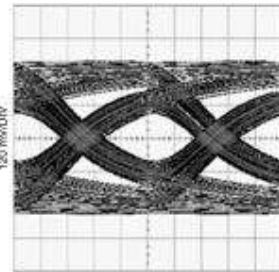
- 1 – **How to extend a chassis' life?** – *Life Extender, Reach extender, Eye Opener*
- 2 – **Active Cable** – *Optimization!*
- 3 – **10G Backplane, PCIe-Gen3, SAS-3** – *Protocol Savvy*

# 1

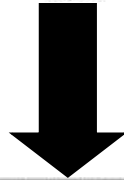
## How to extend a chassis' life?



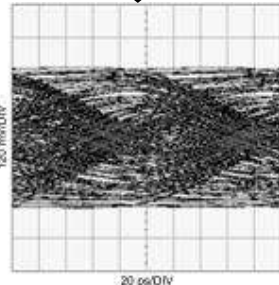
**5 Gbps**



*Double the Data Rate and the Eye closes!*



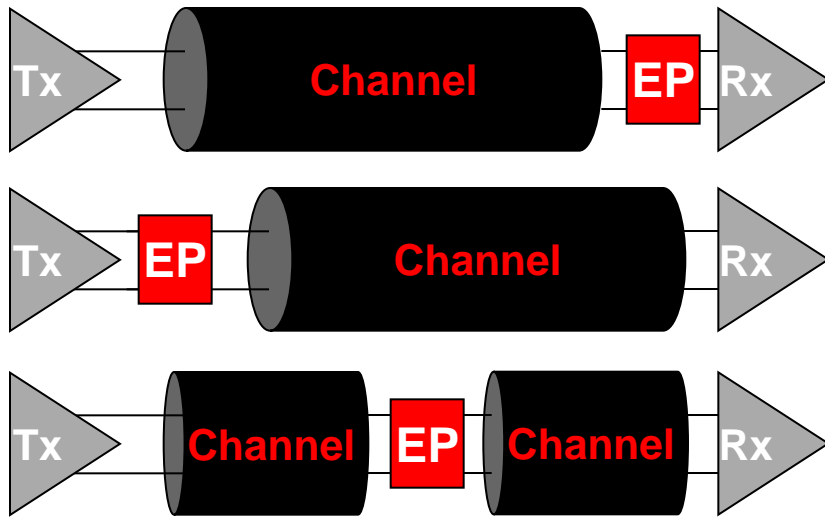
**10 Gbps**



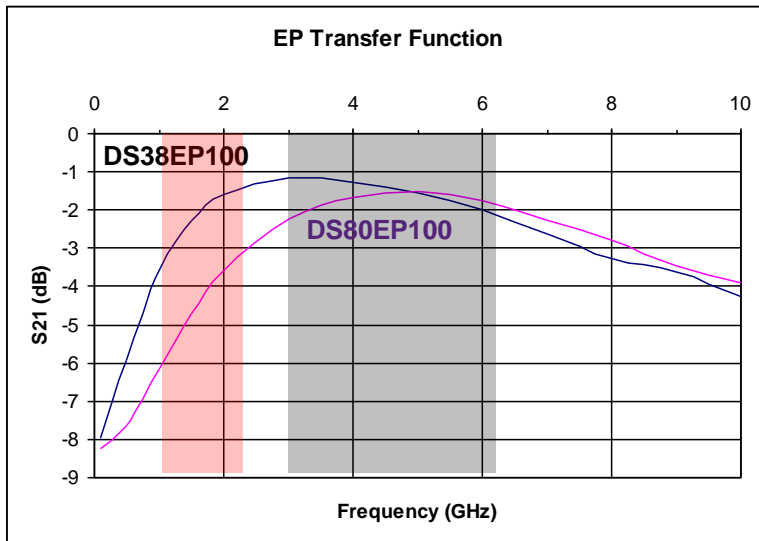
- Loss is a function of channel
  - Trace (e.g. FR4, 6mil, microstrip)
  - Via
  - Connectors
  - Data Rate
- Doubling of Data Rate – huge impact!
- Life Extension of H/W
- But Eye is closed!
  - Jitter 100%
  - Amplitude
- **Open the EYE with a PowerSaver Equalizer Solution**

# 1

## PowerSaver Equalizers – EP Family

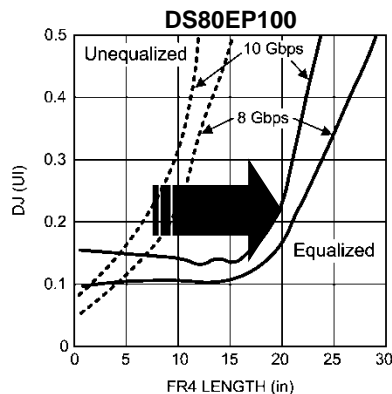
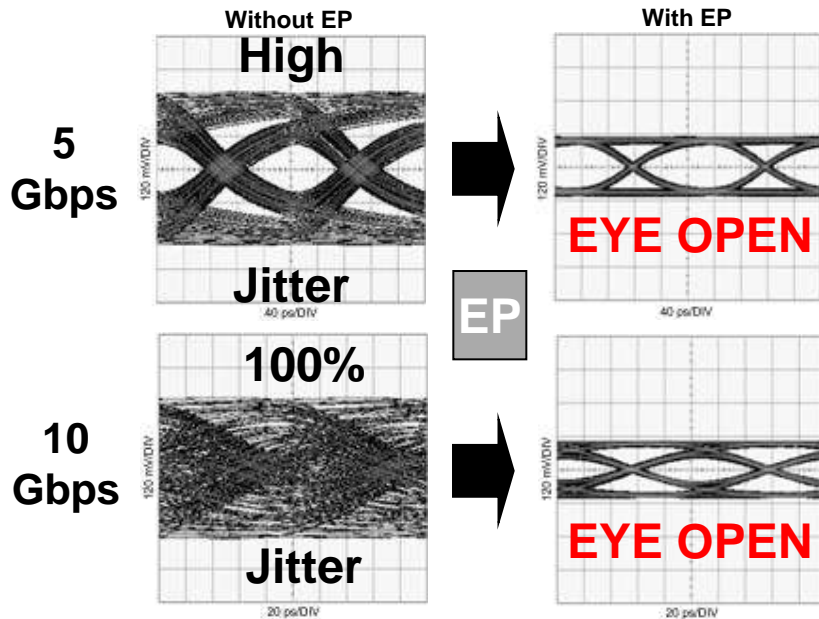


- DS38EP100 (2 to 5Gbps)
- DS80EP100 (5 to 12.5Gbps)
- EPs can be located at **ANY** point in the path
- Small Size (2.2mm x 2.5mm)
- **No Power or GND connection required!**
- **Works with CML, LVPECL, or LVDS signaling**
- **Works with any codes: 8b10b, scrambled, DC....**
- **Bi-directional**
- Economical boost solution that extends the life of a unit!



# 1

# EP Design Considerations

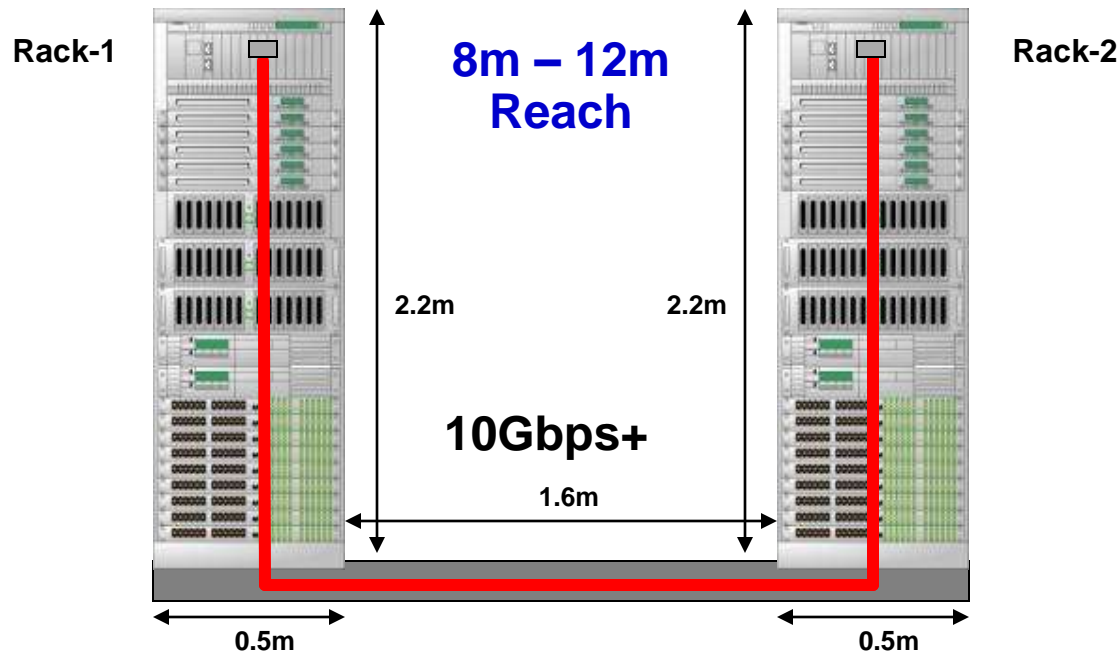


- PowerSaver Equalizers **reduce jitter** and **open the eye** – provides a DE function
- **Will attenuate** the signal (8dB)
  - Must meet RX minimum sensitivity requirement
  - TX optimization – increase VOD (1Vpp) or use Pre-Emphasis – De-Emphasis not recommended
  - Can work with Active EQs  
Can stack but watch attenuation
- **DS38EP100** targeted at:
  - 2 to 5Gbps
  - 40" FR4 6mil microstrip or other
- **DS80EP100** targeted at:
  - 5 to 12Gbps
  - 20" FR4 6mil microstrip or other
- **Extends the Data Rate or Extends the Reach**

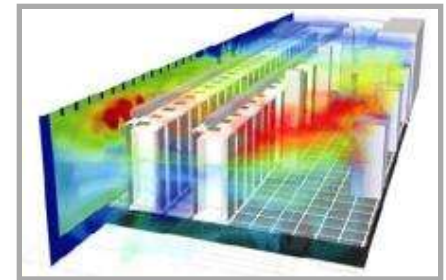
# 2 Active Copper Cables

## *Rack-to-Rack Reach*

How to extends the reach on lower gauge wires to replace fiber for lengths under 15 meters?



**Permit Airflow**



**Installation Flexibility**



# 2

## Data Center & HPC Cabling Solutions *Passive Copper, Active Copper, Active Optical*

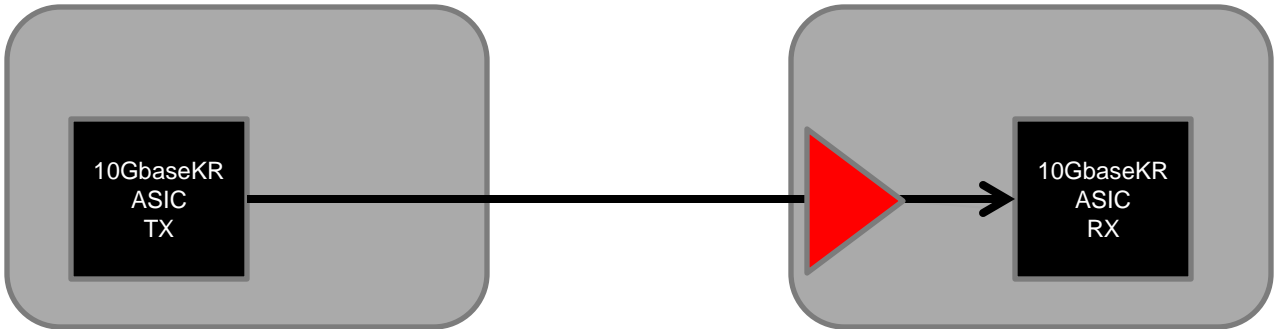
**Passive Copper**  
QSFP : 5m, \$X, 0W

**Active Copper Cables**  
QSFP : 20m, \$3X, 440mW

**Active Optical Cables (AOC)**  
QSFP : 100m, \$6X, 1000mW+

# 3

## 10G Base KR link training optimizes system level signal performance and power between TX and RX ASICs.



Passive (PowerSaver)			<ul style="list-style-type: none"><li>• Passes Link Training</li><li>• Low Power</li><li>• <b>Attenuation impact</b></li></ul>
Limiting Stage			<ul style="list-style-type: none"><li>• <b>Impacts Link Training</b></li></ul>
Linear Stage			<ul style="list-style-type: none"><li>• Passes Link Training</li><li>• Preserves waveshape</li><li>• Preserves Amplitude</li></ul>



# Summary

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# TI Sigcon in the NEWS! (JAN 31, 2012)

The screenshot shows the EE Times website interface. At the top left is the EE Times logo. To the right is a search bar with a 'Search' button and an 'Advanced Search' link. Below the logo is a navigation menu with links for Home, News & Analysis, Business, EE Life, Embedded.com, Design, Products, Education & Training, Events, and Video. On the far right of the menu are 'Sign In' and 'Join' links. The main content area features a large article titled 'DesignCon: Avago, TI hit signal milestones', with the words 'Avago, TI' circled in red. The article includes a large image of signal traces and a text block that reads: 'Claiming milestones in speed, reach and power, Avago announced a 25 Gbit/s serdes and Texas Instruments rolled a family 12.5G signal conditioners at DesignCon. Read Full Story'. To the right of the main article is a sidebar with a 'What's new at EE Times' section containing links for 'EE Times at DesignCon', 'DESIGNCON 2012', 'designwest', and 'EE Buzz DesignCon'. Below this is a 'Recommend us:' section with social media sharing options (Like, Send, Share, Tweet) and a 'Follow EE Times:' section with links for Newsletter, Facebook, Twitter, Google+, and LinkedIn. There is also a 'Download: Digital Edition PDF' link and a 'New!' section for digital editions.

## Signal Conditioning - Repeaters, Retimers and Mux-Buffers

Twice the Reach, Half the Power. Lower Interconnect Cost

TI's signal conditioners for Backplanes, Cables, and Optical Modules combine cutting edge silicon process technology with advanced analog circuit design, delivering the industry's highest signal conditioning performance at the lowest power consumption in a comprehensive portfolio of easy-to-use products.

Family	Repeaters	Retimers	Advanced Retimers	MUX-Buffers
Compatibility	Pin Compatible			
Block Diagram				
Insertion Loss	EQ, DE	EQ, DE	EQ, DE	EQ, DE
Jitter		CDR	CDR	
Crosstalk			DPE	
Applications	<ul style="list-style-type: none"> <li>Active Cables</li> <li>Backplanes</li> </ul>	<ul style="list-style-type: none"> <li>Front Port Optical</li> </ul>	<ul style="list-style-type: none"> <li>Front Port Backplanes</li> </ul>	<ul style="list-style-type: none"> <li>Redundancy Switch</li> </ul>
New Products	<ul style="list-style-type: none"> <li>DS100KR800 10.3 Gbps octal</li> <li>DS100KR401 14.2 Gbps quad</li> </ul>	<ul style="list-style-type: none"> <li>DS125RT410 9.8 to 12.5 Gbps</li> <li>DS110RT410 8.5 to 11.3 Gbps</li> <li>DS100RT410 10.3 Gbps</li> </ul>	<ul style="list-style-type: none"> <li>DS125DF410 9.8 to 12.5 Gbps</li> <li>DS110DF410 8.5 to 11.3 Gbps</li> <li>DS100DF410 10.3 Gbps</li> </ul>	<ul style="list-style-type: none"> <li>DS100MB203 dual 2:1/1:2 up to 11.5 Gbps</li> <li>SN65LVCP114 quad 2:1/1:2 up to 14.2 Gbps</li> </ul>

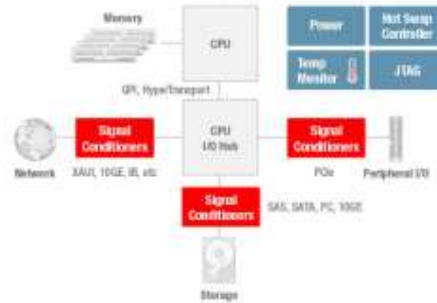
### NEW 12.5 Gbps Retimers — Advanced Signal Conditioning Made Easy

- Pin compatible upgrade between repeaters and retimers - performance when needed!
- Extend reach of 10 Gbps signals over 50+ inches of FR-4 or 20m of 26-AWG copper cable
  - 36 dB input adaptive EQ, 12 dB output de-emphasis (DE)
  - Multi-tap decision feedback equalizer (DFE)
  - Clock and data recovery (CDR) with low-noise LC-VCO
- Reduce bill of materials (BOM) cost, simplify system design
  - Fully adaptive EQ eliminates need for manual link tuning
  - No external reference clock or power filtering required
  - Built-in eye monitor and PRBS generator simplifies system debug
  - Single power supply with integrated noise-rejection filter eliminates need for RF chokes
  - Direct-EEPROM configuration load option eliminates need for software programming
- Repeaters consume 65 mW per channel; retimers with CDR consume 145 mW per channel

### Signal Conditioning at 12.5 Gbps



### Typical Signal Conditioning Application



# NEW SigCon Feature Site!

- Highlights
- Selection Tables
- Video Features / Demos
- System Block Diagrams
- Tools
- Applications Notes
- Design Guides

# Thank You for attending!

## APPENDIX



**TEXAS INSTRUMENTS** [Samples & Purchase Cart](#) | [About TI](#) | [TI Worldwide](#) | [United States](#) | [简体中文](#) | [日本語](#) | [my.TI Login](#)

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### Twice the Reach, Half the Power

Advanced signal conditioning – repeaters & retimers

- Comprehensive portfolio, up to 14.2 Gbps
- Easiest to use, lowest BOM cost
- [Order samples and EVMs today](#)

**TI's Brushless DC Motor Drive Solution** [Learn more](#)

**INA149 Difference Amplifier** [Learn more](#)

# Appendix

時間が余ったときに使用します。

# 4

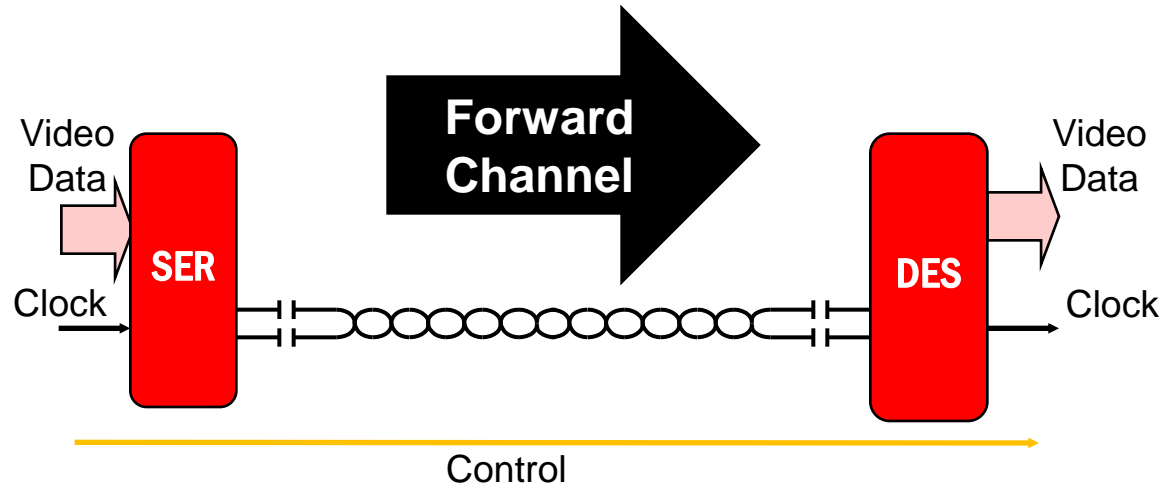
## What is the easiest way to reduce pins, cable bulk, interconnect cost, and GO FAR?

### USE TI's Channel Link II Ser/Des

#### System Benefits

- Reduces Wide Data bus and clock to one pair
- Extends interconnect length
  - Eliminates clock/data skew issues
- SigCon Features for Link extending
  - TX Equalization
  - RX Equalization

#### Block Diagram

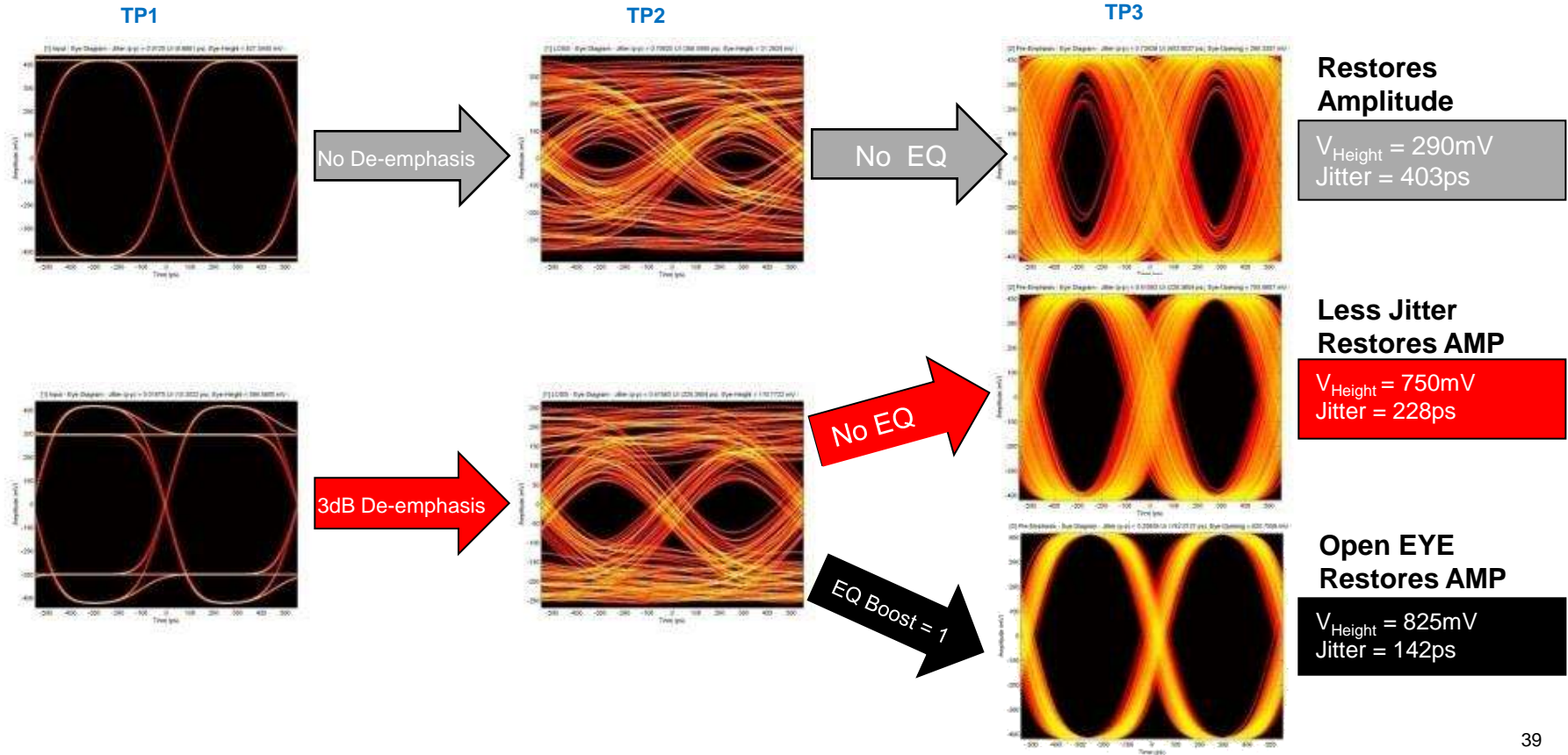
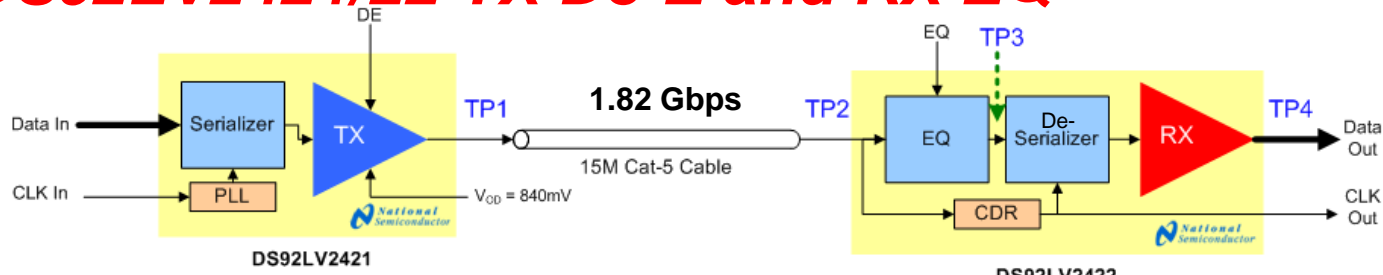


***Data and Embedded Clock use a single pair of wires!***



# 4

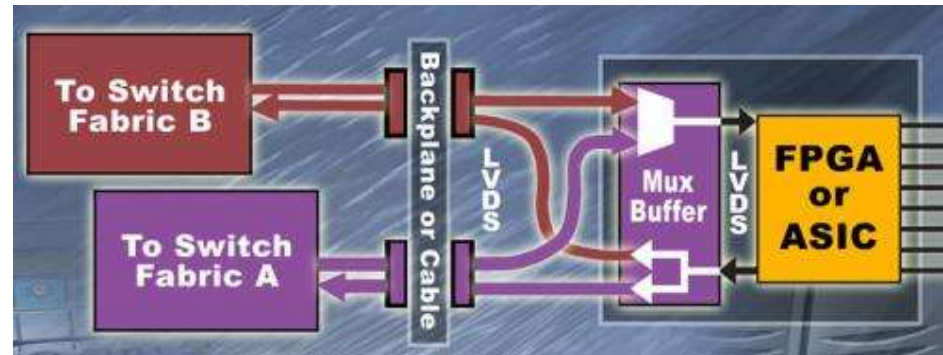
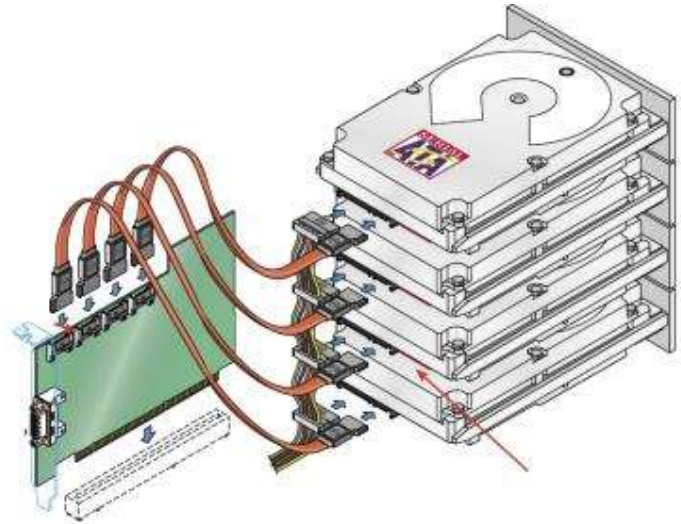
# Channel Link II Signal Conditioning DS92LV2421/22 TX De-E and RX EQ



# 5

## How do I get a high speed signal to two places?

- Multi-drop, Multi-Point usually **limited** to <500 Mbps due to T-Line effects
- Point-to-Point Links are **best** for Signal Integrity when every ps matters!
- Desirable for many applications:
  - Redundancy
  - Fail Over
  - Front / Back Panel Options
- **MUX Buffers provide a 1:2 FANOUT and 2:1 SELECT function**





# 5 Storage: SAS / SATA



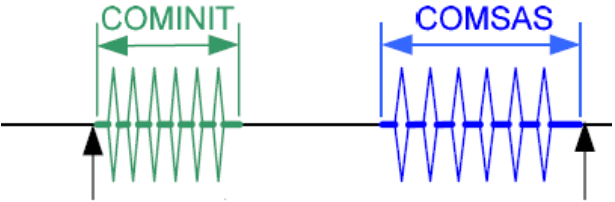
- **SAS 1.0 (3 Gbps), SAS 2.0 (6 Gbps)**
  - Primary target : Enterprise storage
  - Supports multiple initiators
  - Target length 8 meters of cable OR 30" FR4
- **SATA – 6 Gbps, 3 Gbps, 1.5 Gbps**
  - Primary target : Consumer storage
  - Target media length 1 meters of cable
  - eSATA (External SATA) supports 2 meter of cable
- **Both define OOB (Out-of-band) signaling**
  - OOB signal is a pattern of idle times and burst times
    - Idle time : Differential 0 V, No transitions (DC idle)
    - Burst time : Transmitted as a burst of ALIGN(0) primitives
  - Length of idle time distinguishes between OOB signal: COMINIT, COMWAKE, and COMSAS

- Server storage applications:
  - HBA (Host Bus Adapters), servers, storage racks, switches and routers
  - RAID (Redundant Array of Individual Disks) devices/JBODs (Just a Bunch of Disks)



**REDRIVERS cannot block Protocol features!**

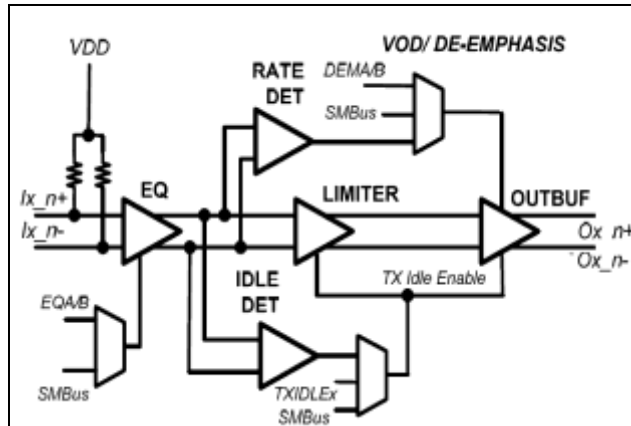
- Link Training
- OBB
- Idle
- LFPS



# 5

## MUX Buffer Magic

DS64MB201



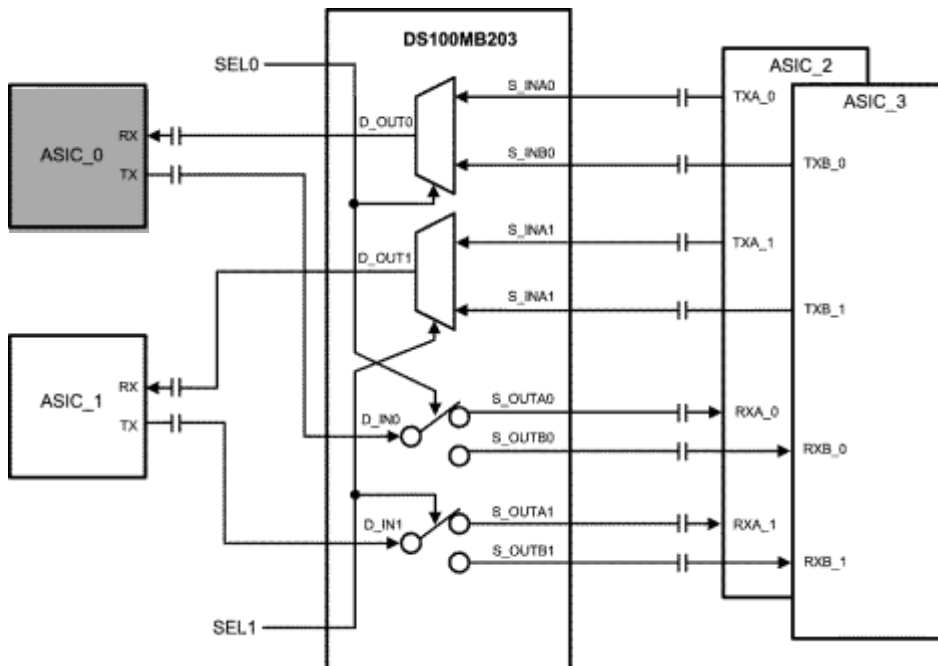
- Signal conditioning on **both input and output stages** for maximum flexibility in physical placement

- Implement system redundancy with **2:1 Multiplex** or **1:2 Fan-out** option

- Extend reach on **back-plane or cable** for SATA/SAS/XAUI/RXAUI/Infiniband etc.

- **DS64MB201 for SATA/SAS and 6Gbps applications**

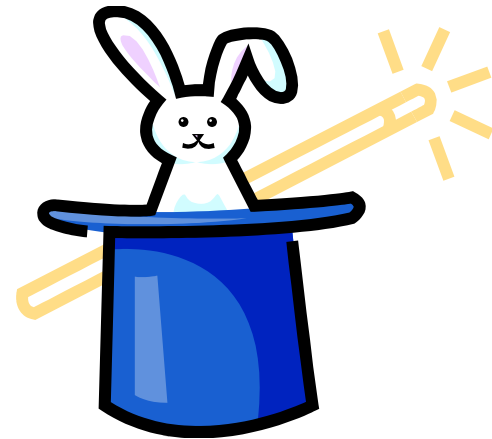
- **DS100MB203 for KR and 10GE 10Gbps applications**



# 6

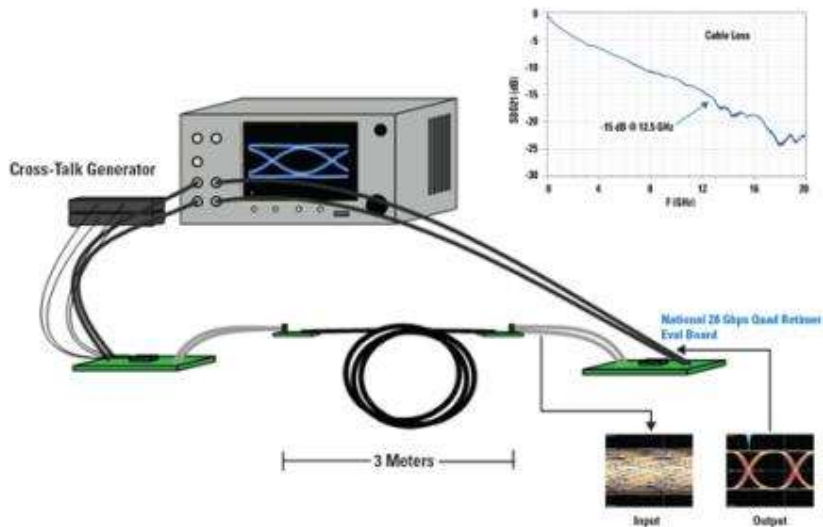
## Are 25/28 Gbps copper Interface even possible?

- **YES** – with TI's BiCMOS 13 Process Technology
- **100GE Applications** –
  - Quad 25G Electrical
  - Quad 28G Electrical (adds overhead for FEC, etc.)
- **An alternative to Optical** (power, post, ease of connections)
- **Challenges:**
  - Edge rate required
  - Open EYE
  - Unit Interval of 40ps to 35.7ps!
  - Interconnect Losses
  - Signal to Noise
  - EMI

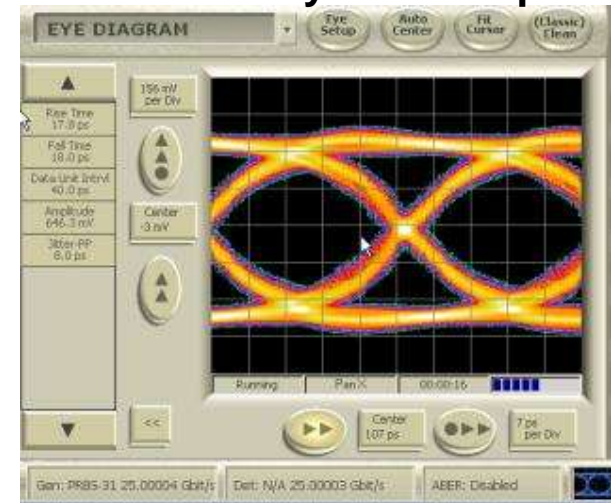


# 6

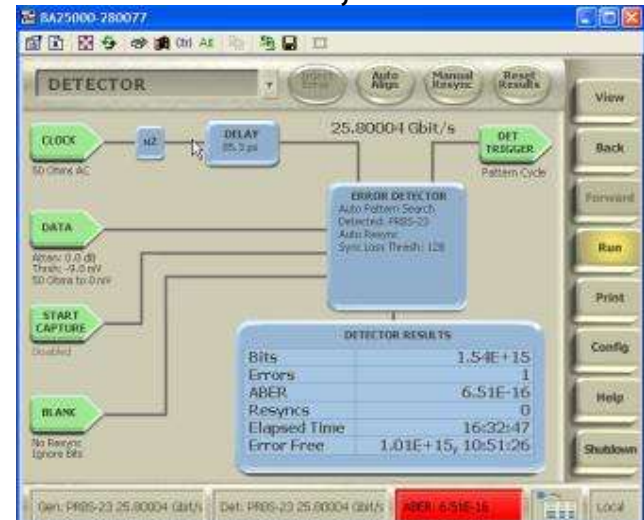
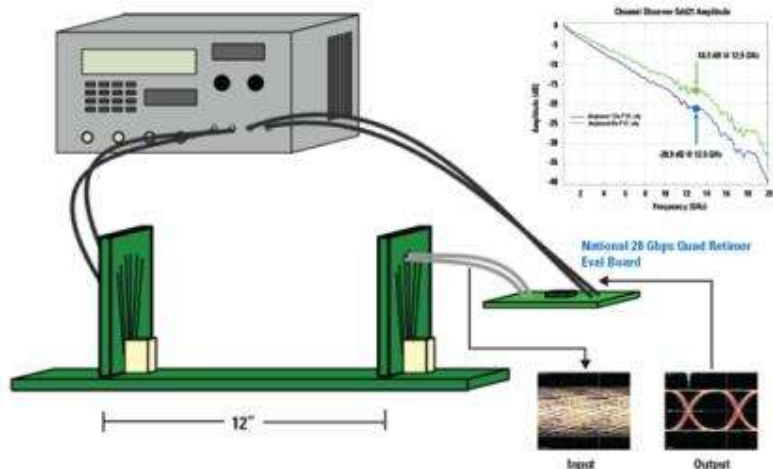
## 25 Gbps Retimers 5m Cable & 20" Backplane Performance



### Recovered Eye – 25 Gbps

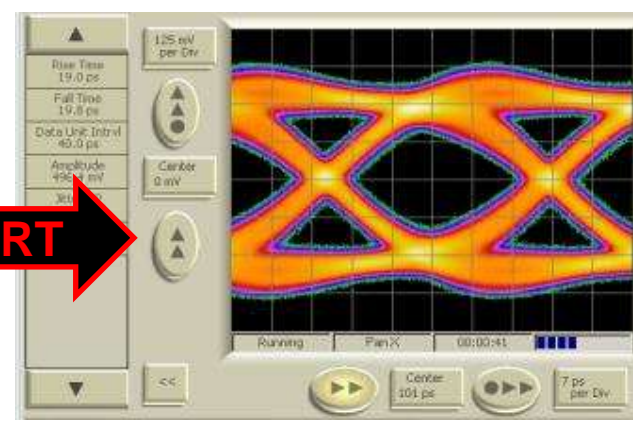
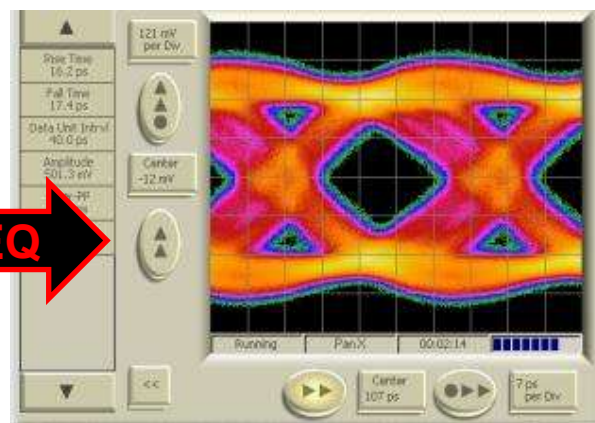
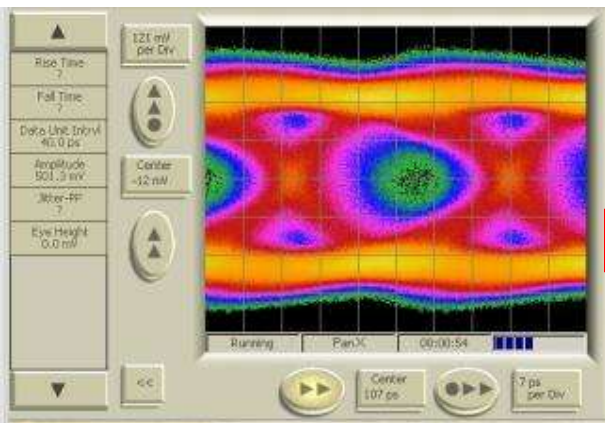


### BER < 1e-15, PRBS-31



# 6

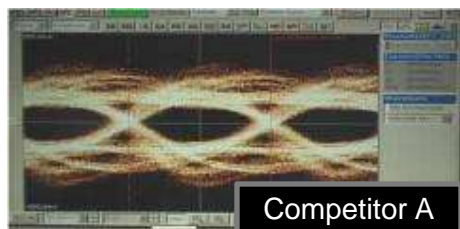
## 25G is real today with TI's BiCMOS13 >100GHz process



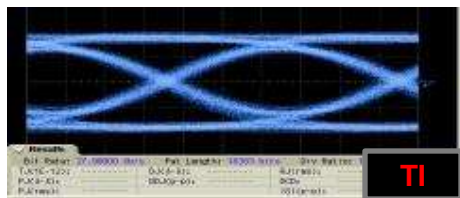
Un-equalized data after a 7.5inch stripline and 2 meters of cable at 25Gbps

Equalized data after a 7.5inch stripline and 2 meters of cable at 25Gbps

Re-timed data after a 7.5inch stripline and 2 meters of cable at 25G

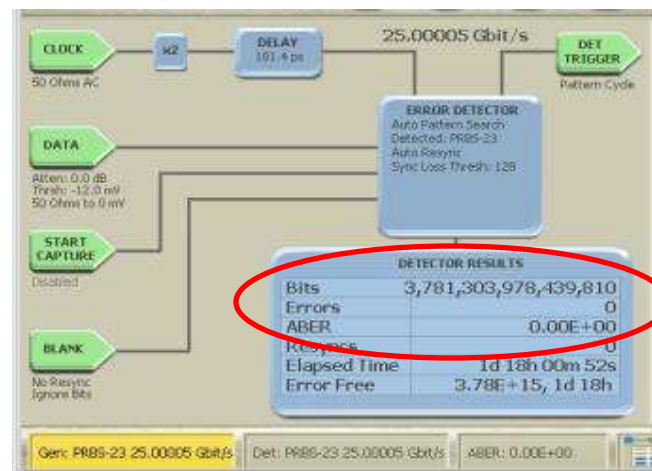


Competitor A



TI

- 25/28 Gbps
- Advanced SigCon
- Low Power
- OPEN EYE
- Zero Error



Zero BER after 1day and 18Hrs  
**3.7 Peta-bits !**